ALPHA & OMEGA SEMICONDUCTOR

AO4936

Asymmetric Dual N-Channel Enhancement Mode Field Effect Transistor

SRFET ™

General Description

The AO4936/L uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A monolithically integrated Schottky diode in parallel with the synchronous MOSFET to boost efficiency further.

AO4936 and AO4936L are electrically identical.

-RoHS Compliant

-AO4936L is Halogen Free

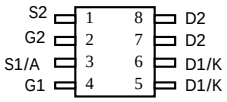
Features

FET1	FET2	
V_{DS} (V) = 30V	V_{DS}(V) = 30V	
I_D = 8.8A	I_D=8.5A	(V_{GS} = 10V)
$R_{DS(ON)}$ < 16mΩ	< 18mΩ	(V_{GS} = 10V)
$R_{DS(ON)}$ < 22mΩ	< 28mΩ	(V_{GS} = 4.5V)

UIS TESTED!

Rg,Ciss,Coss,Crss Tested

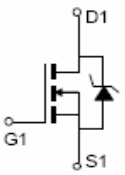
SOIC-8



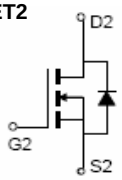
SRFET ™

Soft **R**ecovery MOS**FET**: Integrated Schottky Diode

FET1



FET2



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max FET1		Max FET2		Units
			10 sec	Steady-State	10 sec	Steady-State	
Drain-Source Voltage		V_{DS}	30		30		V
Gate-Source Voltage		V_{GS}	±20		±20		V
Continuous Drain Current [AF]	T_A=25°C	I_{DSM}	8.8	6.7	8.5	6.4	A
	T_A=70°C		7.1	5.3	6.8	5.1	
Pulsed Drain Current [B]		I_{DM}	60		40		A
Avalanche Current [B]		I_{AR}	21		16		A
Repetitive avalanche energy L=0.3mH [B]		E_{AR}	66		38		mJ
Power Dissipation[A]	T_A=25°C	P_{DSM}	2	1.1	2	1.1	W
	T_A=70°C		1.3	0.7	1.3	0.7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		-55 to 150		°C

Thermal Characteristics FET1(Intergrated Schottky Diode)

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		74	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	32	40	°C/W

Thermal Characteristics FET2

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		74	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	32	40	°C/W

FET1(Intergrated Schottky Diode) Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.1	mA
		T_J=125°C			20	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			0.1	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.3	1.65	2	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8.8A		13.3	16	mΩ
		T_J=125°C		20.0	25	
		V_{GS}=4.5V, I_D=7A		17.7	22	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8.8A		37		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.41	0.5	V
I_S	Maximum Body-Diode + Schottky Continuous Current				3.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1267	1600	pF
C_{oss}	Output Capacitance			308		pF
C_{rss}	Reverse Transfer Capacitance			118		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.3	2.0	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	VGS=10V, VDS=15V, ID=8.8A		21	30	
Q_g(4.5V)	Total Gate Charge			10.4		nC
Q_{gs}	Gate Source Charge			3.0		nC
Q_{gd}	Gate Drain Charge			3.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.7Ω, R_{GEN}=3Ω		5.2		ns
t_r	Turn-On Rise Time			3.8		ns
$t_{D(off)}$	Turn-Off DelayTime			21.2		ns
t_f	Turn-Off Fall Time			4.4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8.8A, dI/dt=300A/µs		11.2	15	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8.8A, dI/dt=300A/µs		10.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. The current rating is based on the t≤ 10s thermal resistance rating.

Rev 2: May. 2008

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

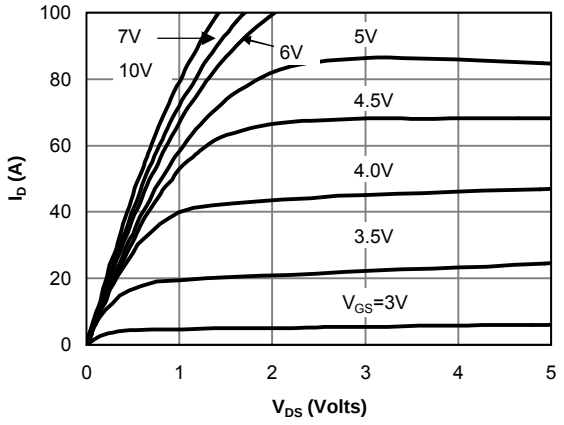


Figure 1: On-Region Characteristics

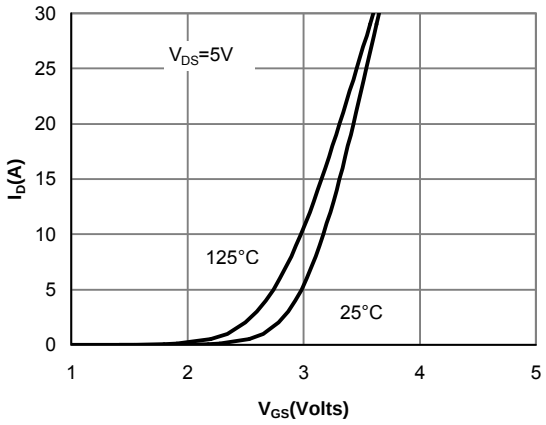


Figure 2: Transfer Characteristics

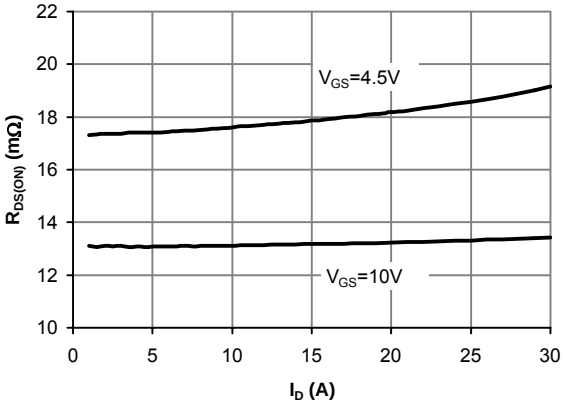


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

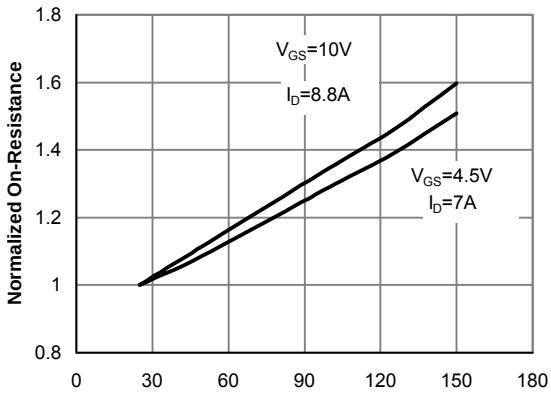


Figure 4: On-Resistance vs. Junction Temperature

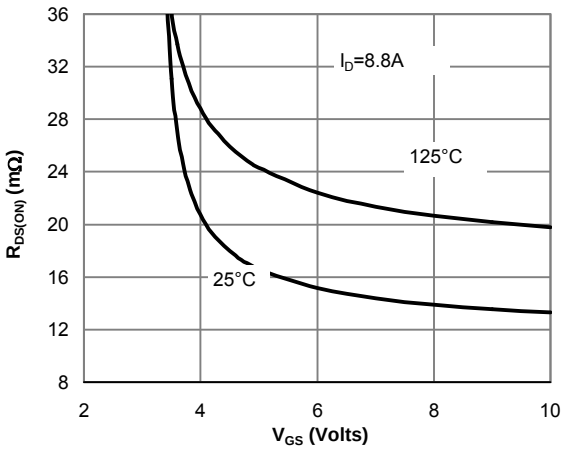


Figure 5: On-Resistance vs. Gate-Source Voltage

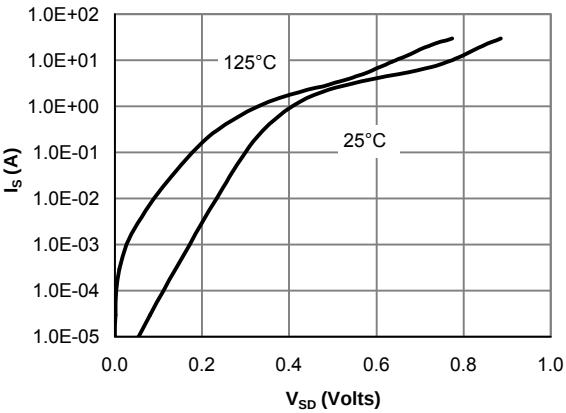


Figure 6: Body-Diode Characteristics

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

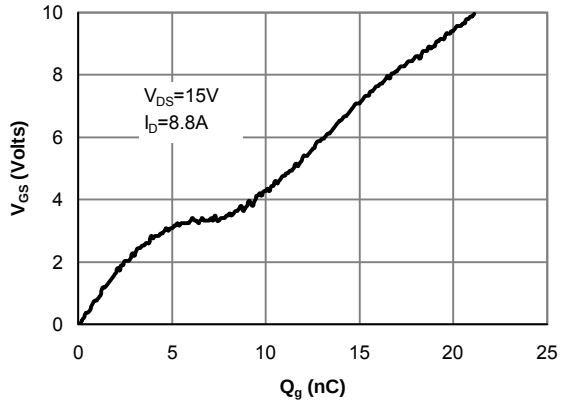


Figure 7: Gate-Charge Characteristics

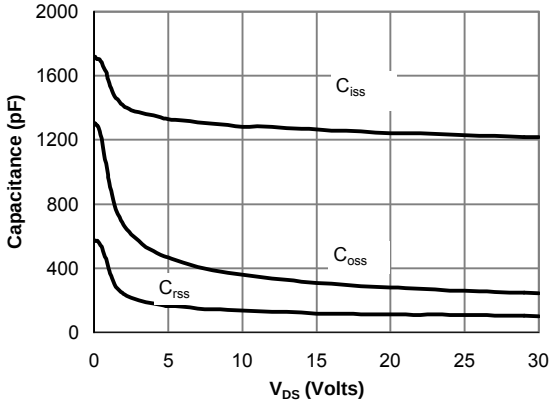


Figure 8: Capacitance Characteristics

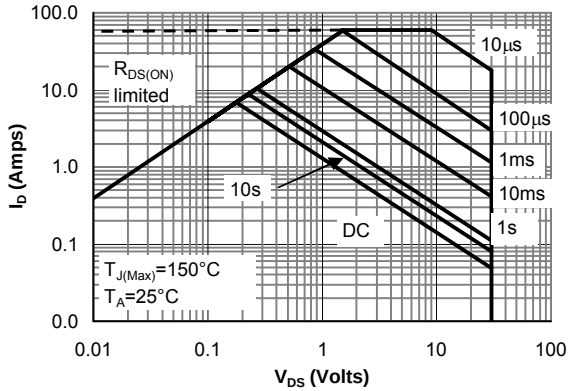


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

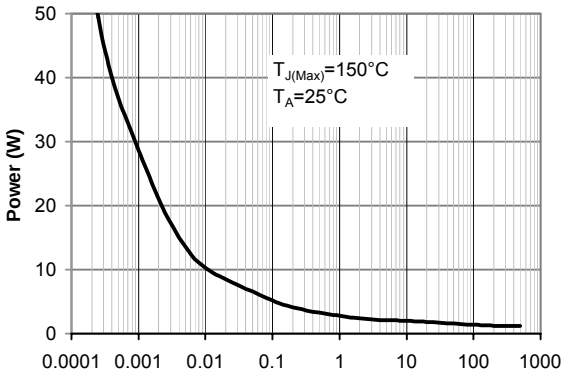


Figure10: Single Pulse Power Rating Junction-to-Ambient (Note E)

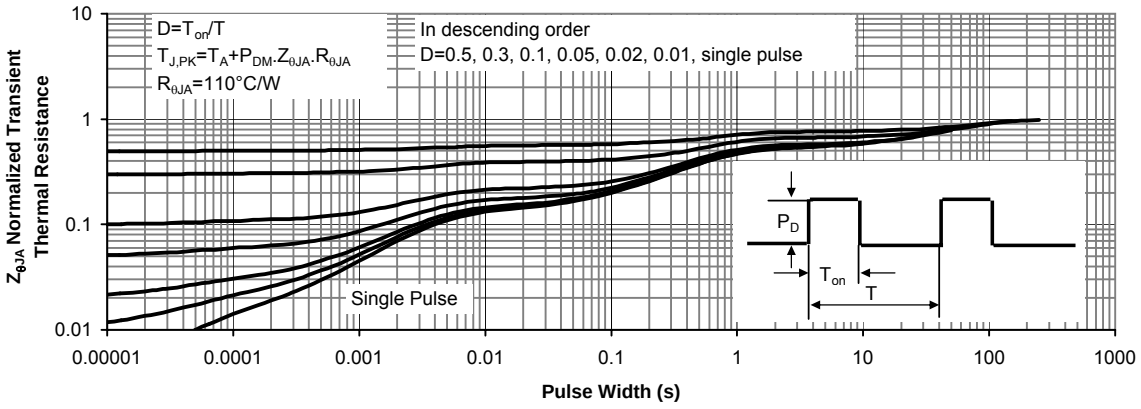


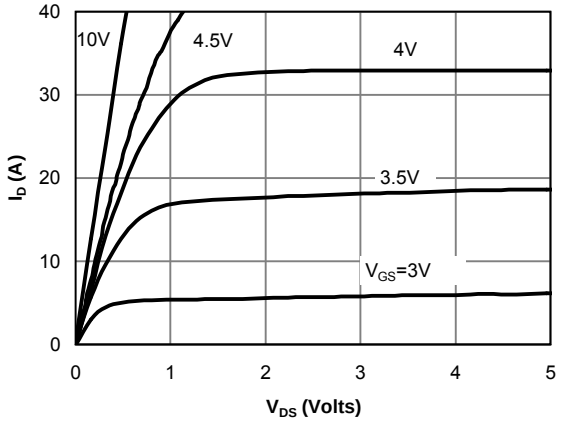
Figure 11: Normalized Maximum Transient Thermal Impedance

FET2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.65	2.3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8.5A		15	18	mΩ
		T_J=125°C		21	27	
		V_{GS}=4.5V, I_D=7A		21.8	28	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8.5A		23		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		955	1250	pF
C_{oss}	Output Capacitance			145		pF
C_{rss}	Reverse Transfer Capacitance			112		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.5	0.85	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=8.5A		17	24	nC
Q_g(4.5V)	Total Gate Charge			9	12	nC
Q_{gs}	Gate Source Charge			3.4		nC
Q_{gd}	Gate Drain Charge			4.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.75Ω, R_{GEN}=3Ω		5		ns
t_r	Turn-On Rise Time			6		ns
$t_{D(off)}$	Turn-Off DelayTime			19		ns
t_f	Turn-Off Fall Time			4.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8.5A, dI/dt=100A/µs		16.7	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8.5A, dI/dt=100A/µs		6.7		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
F. The current rating is based on the ≤ 10s thermal resistance rating.
Rev 2: May. 2008

FET2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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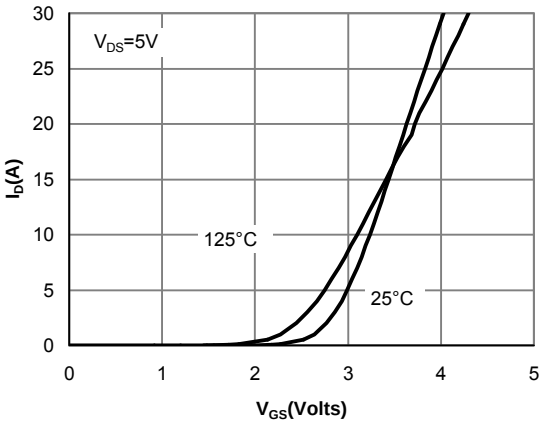
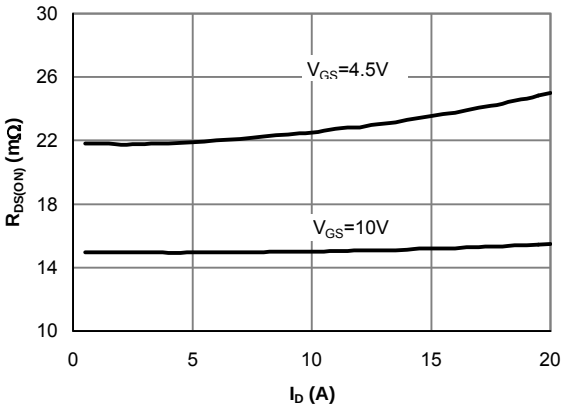


Figure 2: Transfer Characteristics



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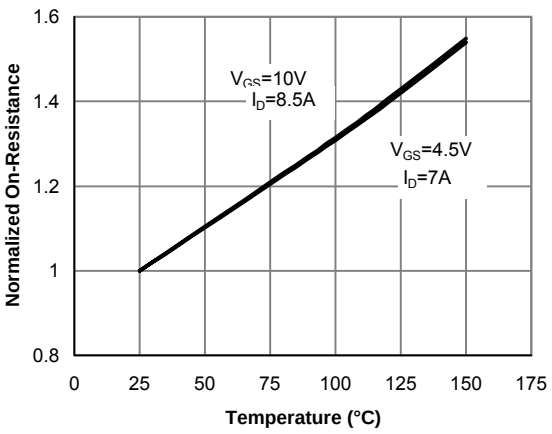

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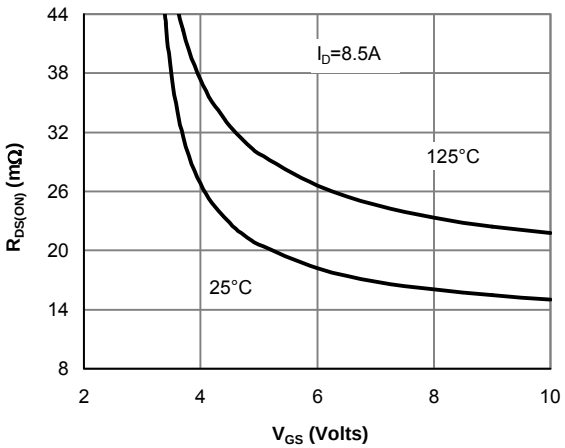

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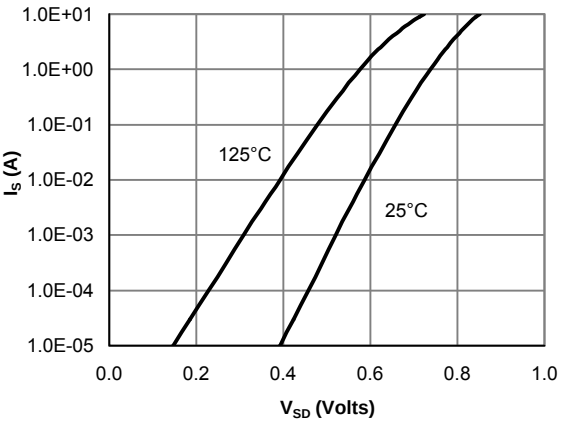

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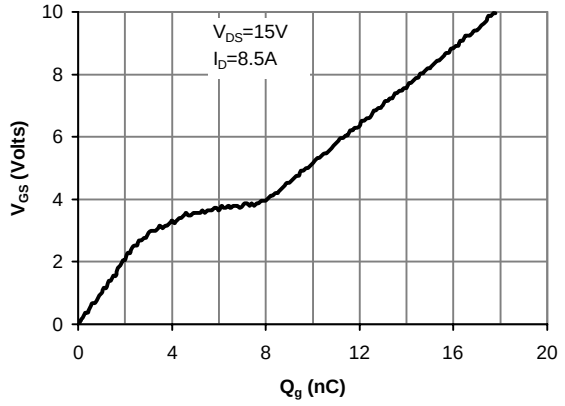

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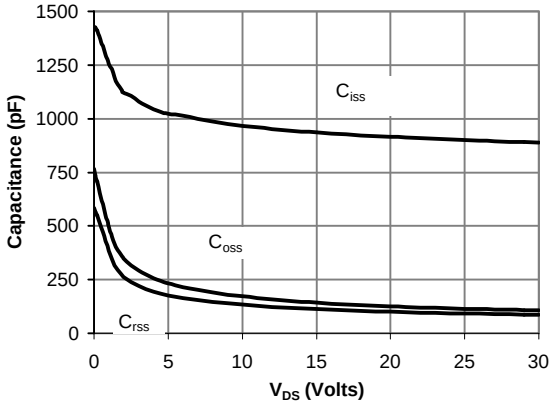

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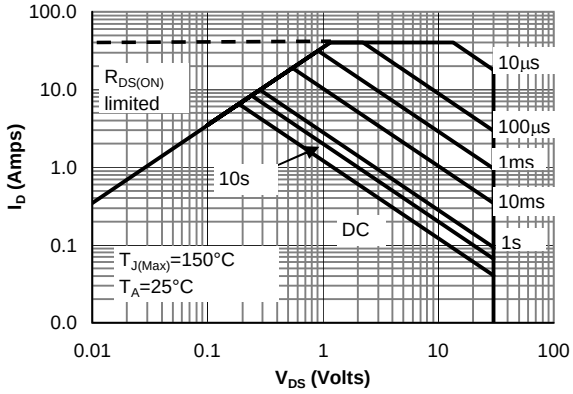

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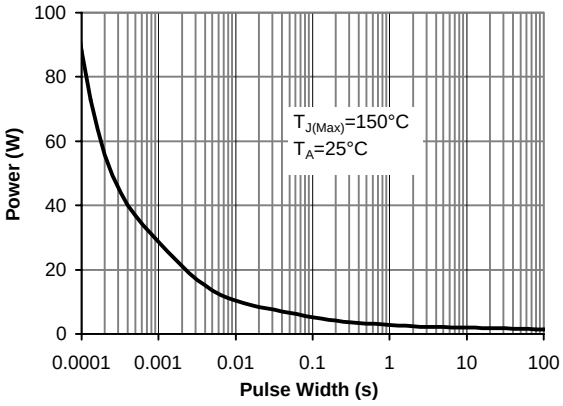

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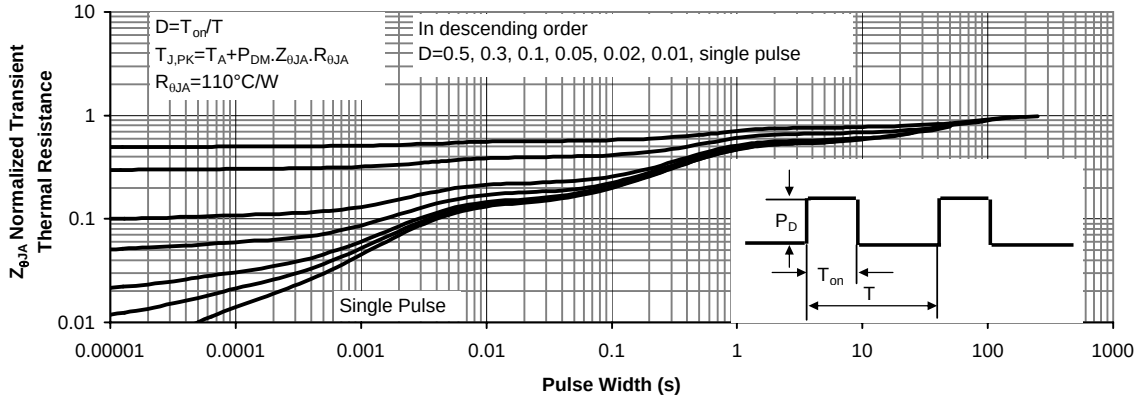

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