

# FAN7371

## High-Current High-Side Gate Drive IC

### Features

- Floating Channel for Bootstrap Operation to +600V
- 4A/4A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- 3.3V and 5V Input Logic Compatible
- Output In-phase with Input Signal
- Under- Voltage Lockout for  $V_{BS}$
- 25V Shunt Regulator on  $V_{DD}$  and  $V_{BS}$
- 8-Lead Small Outline Package (SOP)

### Applications

- High-Speed Gate Driver
- Sustain Switch Driver in PDP Application
- Energy-Recovery Circuit Switch Driver in PDP Application
- High-Power Buck Converter
- Motor Drive Inverter

### Description

The FAN7371 is a monolithic high-side gate drive IC, which can drive high-speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to  $V_S = -9.8V$  (typical) for  $V_{BS} = 15V$ .

The UVLO circuit prevents malfunction when  $V_{BS}$  is lower than the specified threshold voltage.

The high-current and low-output voltage drop feature makes this device suitable for sustain and energy recovery circuit switches driver in the Plasma Display Panel application, motor drive inverter, switching power supply, and high-power DC-DC converter applications.

8-SOP



### Ordering Information

| Part Number | Package | Pb-Free | Operating Temperature Range | Packing Method |
|-------------|---------|---------|-----------------------------|----------------|
| FAN7371M    | 8-SOP   | Yes     | -40°C ~ 125°C               | TUBE           |
| FAN7371MX   |         |         |                             | TAPE & REEL    |

**Note:**

- 1 These devices passed wave soldering test by JESD22A-111.

Typical Application Diagrams

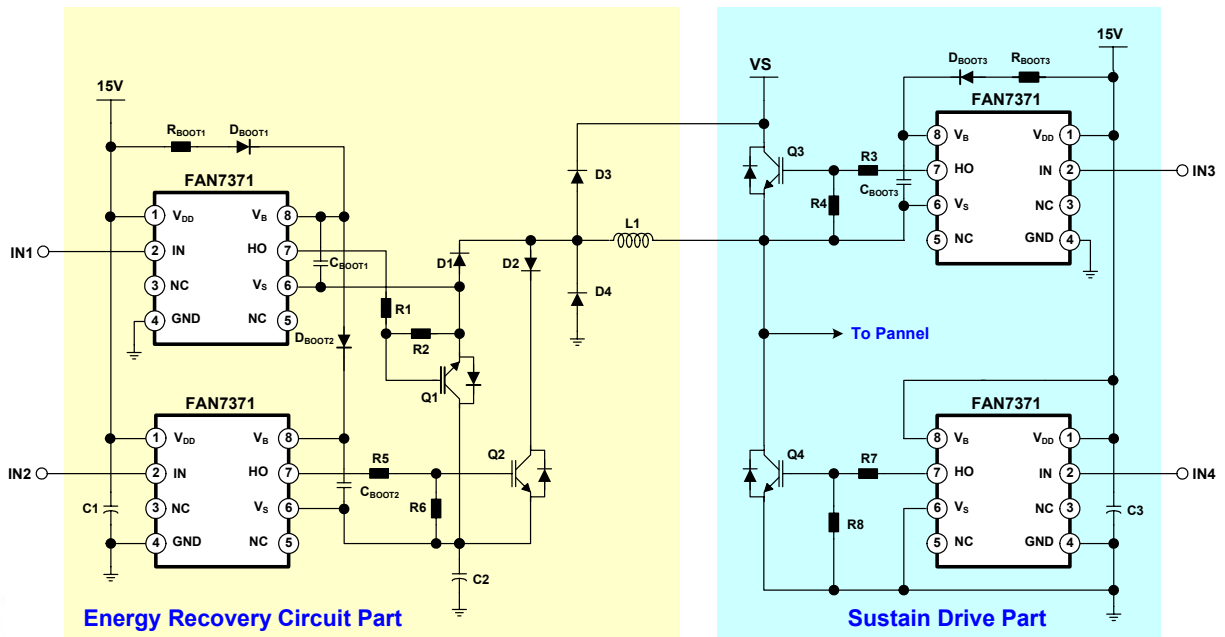


Figure 1. Floated Bidirectional Switch and Half-Bridge Driver: PDP application

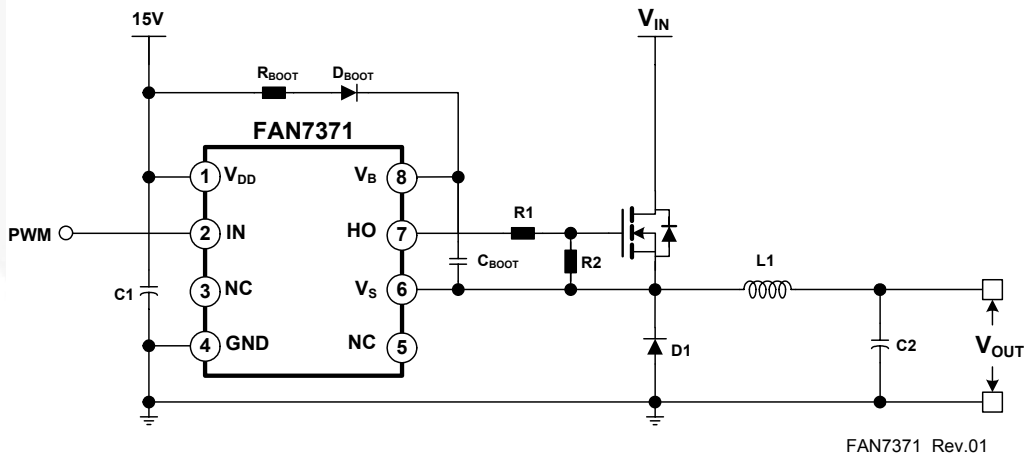


Figure 2. Step-Down (Buck) DC-DC Converter Application

### Internal Block Diagram

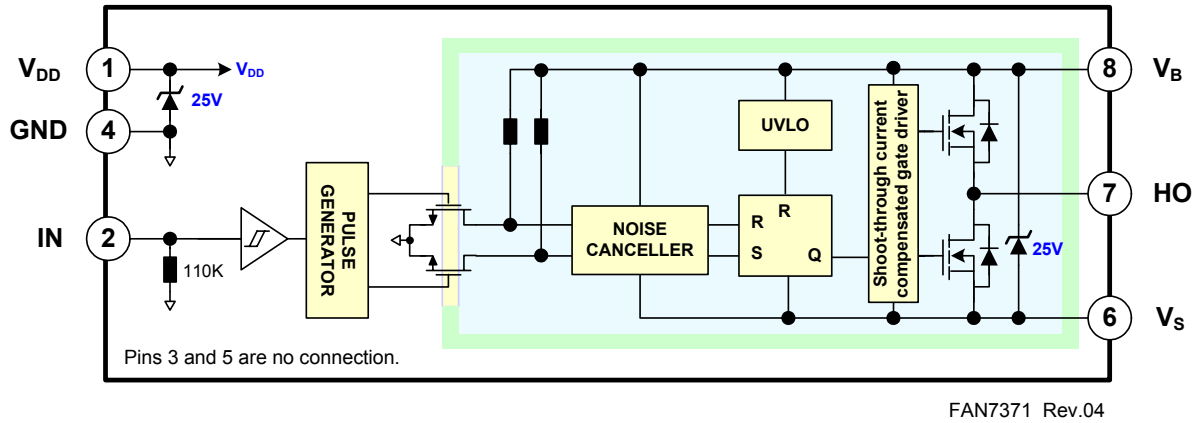


Figure 3. Functional Block Diagram

### Pin Configuration

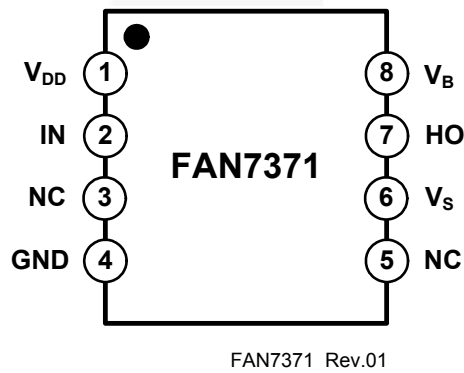


Figure 4. Pin Configuration (Top View)

### Pin Definitions

| Pin # | Name            | Description                                  |
|-------|-----------------|--|
| 1     | V <sub>DD</sub> | Supply Voltage                               |
| 2     | IN              | Logic Input for High-Side Gate Driver Output |
| 3     | NC              | No Connection                                |
| 4     | GND             | Ground                                       |
| 5     | NC              | No Connection                                |
| 6     | V <sub>S</sub>  | High-Voltage Floating Supply Return          |
| 7     | HO              | High-Side Driver Output                      |
| 8     | V <sub>B</sub>  | High-Side Floating Supply                    |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A=25^{\circ}\text{C}$  unless otherwise specified.

| Symbol        | Characteristics                                  | Min.              | Max.           | Unit                        |
|---------------|--|-------------------|----------------|-----------------------------|
| $V_S$         | High-Side Floating Offset Voltage                | $V_B - V_{SHUNT}$ | $V_B + 0.3$    | V                           |
| $V_B$         | High-Side Floating Supply Voltage <sup>(2)</sup> | -0.3              | 625.0          | V                           |
| $V_{HO}$      | High-Side Floating Output Voltage                | $V_S - 0.3$       | $V_B + 0.3$    | V                           |
| $V_{DD}$      | Low-Side and Logic Supply Voltage <sup>(2)</sup> | -0.3              | $V_{SHUNT}$    | V                           |
| $V_{IN}$      | Logic Input Voltage                              | -0.3              | $V_{DD} + 0.3$ | V                           |
| $dV_S/dt$     | Allowable Offset Voltage Slew Rate               |                   | $\pm 50$       | V/ns                        |
| $P_D$         | Power Dissipation <sup>(3, 4, 5)</sup>           |                   | 0.625          | W                           |
| $\theta_{JA}$ | Thermal Resistance                               |                   | 200            | $^{\circ}\text{C}/\text{W}$ |
| $T_{JMAX}$    | Maximum Junction Temperature                     |                   | 150            | $^{\circ}\text{C}$          |
| $T_{STG}$     | Storage Temperature                              | -55               | 150            | $^{\circ}\text{C}$          |

### Notes:

- This IC contains a shunt regulator on  $V_{DD}$  and  $V_{BS}$  with a normal breakdown voltage of 25V. Please note that this supply pin should not be driven by a low-impedance voltage source greater than the  $V_{SHUNT}$  specified in the Electrical Characteristics section
- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:  
JESD51-2: Integral circuits thermal test method environmental conditions, natural convection, and  
JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
- Do not exceed power dissipation ( $P_D$ ) under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol   | Parameter                                | Min.         | Max.       | Unit               |
|----------|--|--------------|------------|--------------------|
| $V_B$    | High-Side Floating Supply Voltage        | $V_S + 10$   | $V_S + 20$ | V                  |
| $V_S$    | High-Side Floating Supply Offset Voltage | $6 - V_{DD}$ | 600        | V                  |
| $V_{HO}$ | High-Side Output Voltage                 | $V_S$        | $V_B$      | V                  |
| $V_{IN}$ | Logic Input Voltage                      | GND          | $V_{DD}$   | V                  |
| $V_{DD}$ | Supply Voltage                           | 10           | 20         | V                  |
| $T_A$    | Operating Ambient Temperature            | -40          | 125        | $^{\circ}\text{C}$ |

## Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})=15.0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to GND. The  $V_O$  and  $I_O$  parameters are relative to  $V_S$  and are applicable to the respective output HO.

| Symbol                             | Characteristics  | Test Condition                                 | Min. | Typ. | Max. | Unit       |
|------------------------------------|--|--|------|------|------|------------|
| <b>POWER SUPPLY SECTION</b>        |  |  |      |      |      |            |
| $I_{QDD}$                          | Quiescent $V_{DD}$ Supply Current                                    | $V_{IN}=0V$ or $5V$                            |      | 25   | 70   | $\mu A$    |
| $I_{PDD}$                          | Operating $V_{DD}$ Supply Current                                    | $f_{IN}=20KHz$ , No Load                       |      | 35   | 100  | $\mu A$    |
| <b>BOOTSTRAPPED SUPPLY SECTION</b> |  |  |      |      |      |            |
| $V_{BSUV+}$                        | $V_{BS}$ Supply Under-Voltage Positive Going Threshold Voltage       | $V_{IN}=0V$ , $V_{BS}=\text{Sweep}$            | 8.2  | 9.2  | 10.2 | V          |
| $V_{BSUV-}$                        | $V_{BS}$ Supply Under-Voltage Negative Going Threshold Voltage       | $V_{IN}=0V$ , $V_{BS}=\text{Sweep}$            | 7.5  | 8.5  | 9.5  | V          |
| $V_{BSHYS}$                        | $V_{BS}$ Supply Under-Voltage Lockout Hysteresis Voltage             | $V_{IN}=0V$ , $V_{BS}=\text{Sweep}$            |      | 0.7  |      | V          |
| $I_{LK}$                           | Offset Supply Leakage Current  | $V_B=V_S=600V$                                 |      |      | 10   | $\mu A$    |
| $I_{QBS}$                          | Quiescent $V_{BS}$ Supply Current                                    | $V_{IN}=0V$ or $5V$                            |      | 60   | 120  | $\mu A$    |
| $I_{PBS}$                          | Operating $V_{BS}$ Supply Current                                    | $C_{LOAD}=1000pF$ , $f_{IN}=20KHz$ , rms value |      | 1.0  | 2.8  | mA         |
| <b>SHUNT REGULATOR SECTION</b>     |  |  |      |      |      |            |
| $V_{SHUNT}$                        | $V_{DD}$ and $V_{BS}$ Shunt Regulator Clamping Voltage               | $I_{SHUNT}=5mA$                                | 24   | 25   |      | V          |
| <b>INPUT LOGIC Section</b>         |  |  |      |      |      |            |
| $V_{IH}$                           | Logic "1" Input Voltage  |  | 2.5  |      |      | V          |
| $V_{IL}$                           | Logic "0" Input Voltage  |  |      |      | 0.8  | V          |
| $I_{IN+}$                          | Logic Input High Bias Current  | $V_{IN}=5V$                                    |      | 45   | 70   | $\mu A$    |
| $I_{IN-}$                          | Logic Input Low Bias Current   | $V_{IN}=0V$                                    |      |      | 2    | $\mu A$    |
| $R_{IN}$                           | Input Pull-down Resistance   |  | 70   | 110  |      | K $\Omega$ |
| <b>GATE DRIVER OUTPUT SECTION</b>  |  |  |      |      |      |            |
| $V_{OH}$                           | High-Level Output Voltage ( $V_{BIAS} - V_O$ )                       | No Load  |      |      | 1.2  | V          |
| $V_{OL}$                           | Low-Level Output Voltage   | No Load  |      |      | 30   | mV         |
| $I_{O+}$                           | Output High, Short-Circuit Pulsed Current <sup>(6)</sup>             | $V_{HO}=0V$ , $V_{IN}=5V$ , $PW \leq 10\mu s$  | 3.0  | 4.0  |      | A          |
| $I_{O-}$                           | Output Low, Short-Circuit Pulsed Current <sup>(6)</sup>              | $V_{HO}=15V$ , $V_{IN}=0V$ , $PW \leq 10\mu s$ | 3.0  | 4.0  |      | A          |
| $V_S$                              | Allowable Negative $V_S$ pin Voltage for IN Signal Propagation to HO |  |      | -9.8 | -7.0 | V          |

### Note:

6 These parameters guaranteed by design.

## Dynamic Electrical Characteristics

$V_{DD}=V_{BS}=15V$ ,  $GND=0V$ ,  $C_{LOAD}=1000pF$ ,  $T_A=25^\circ C$ , unless otherwise specified.

| Symbol    | Parameter                       | Conditions | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------|------------|------|------|------|------|
| $t_{on}$  | Turn-on Propagation Delay Time  | $V_S=0V$   |      | 150  | 210  | ns   |
| $t_{off}$ | Turn-off Propagation Delay Time | $V_S=0V$   |      | 150  | 210  | ns   |
| $t_r$     | Turn-on Rise Time               |            |      | 25   | 50   | ns   |
| $t_f$     | Turn-off Fall Time              |            |      | 15   | 40   | ns   |

Typical Characteristics

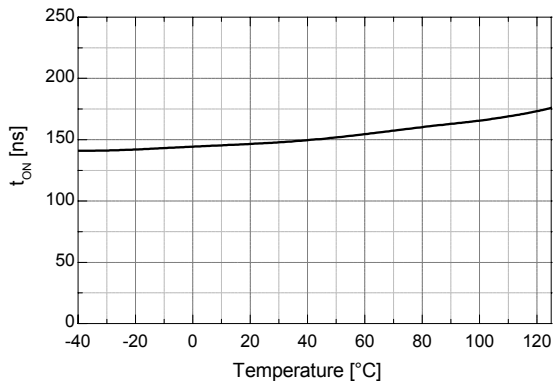


Figure 5. Turn-on Propagation Delay vs. Temp.

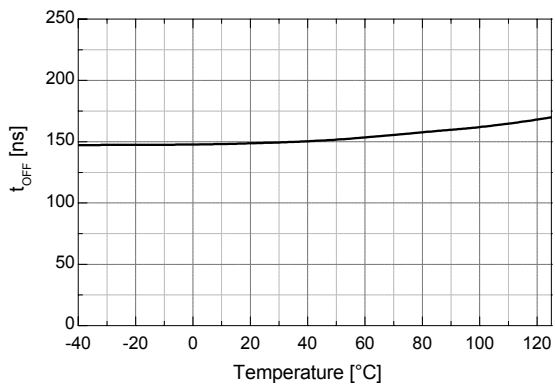


Figure 6. Turn-off Propagation Delay vs. Temp.

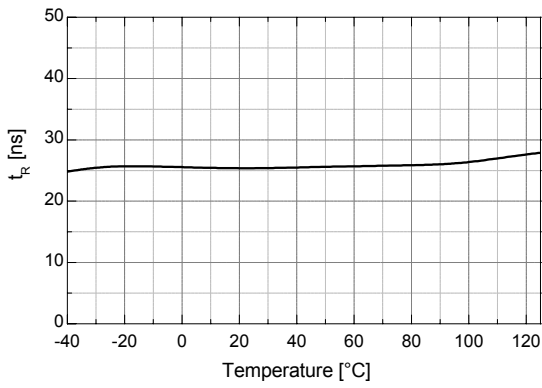


Figure 7. Turn-on Rise Time vs. Temp.

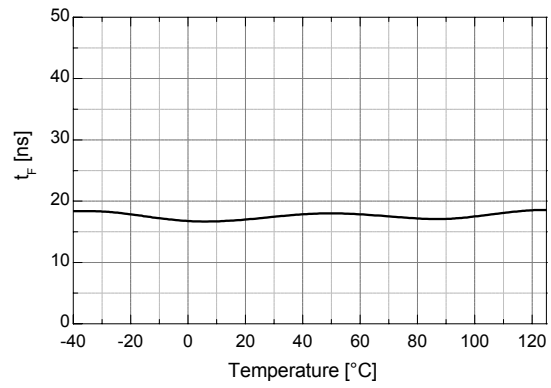


Figure 8. Turn-off Fall Time vs. Temp.

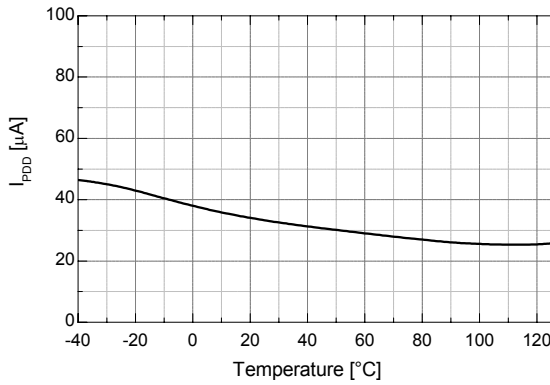


Figure 9. Operating V<sub>DD</sub> Supply Current vs. Temp.

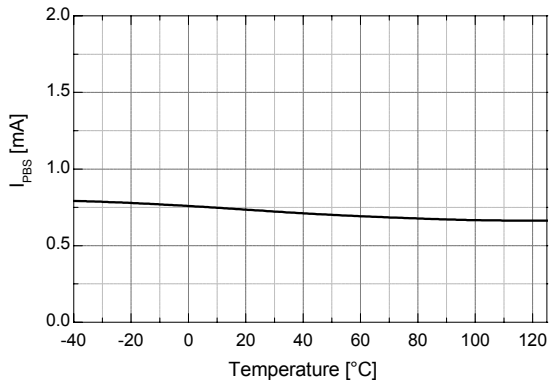
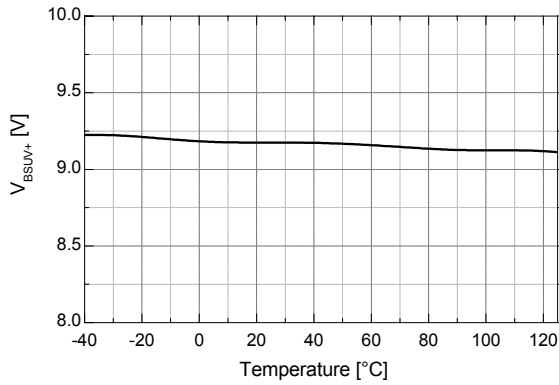
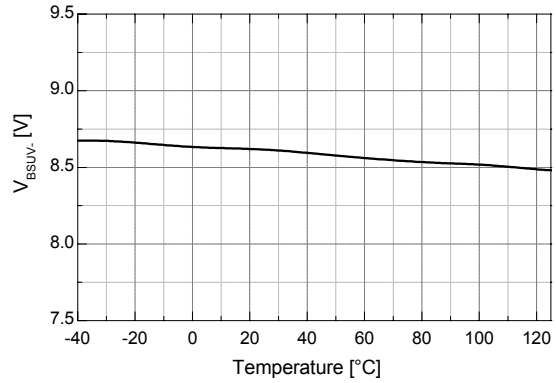


Figure 10. Operating V<sub>BS</sub> Supply Current vs. Temp.

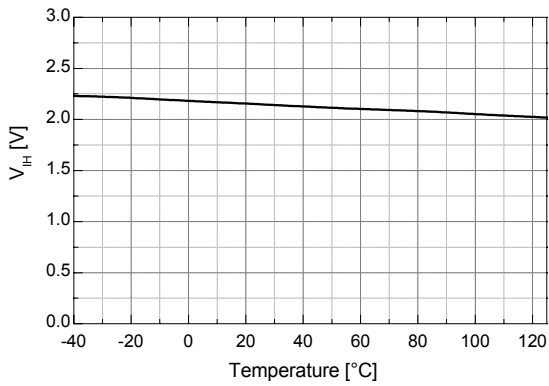
**Typical Characteristics (Continued)**



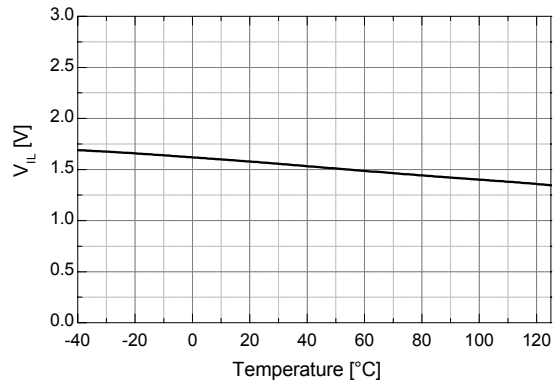
**Figure 11.  $V_{BS}$  UVLO+ vs. Temp.**



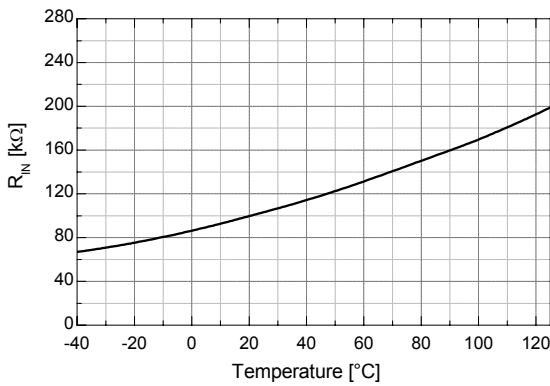
**Figure 12.  $V_{BS}$  UVLO- vs. Temp.**



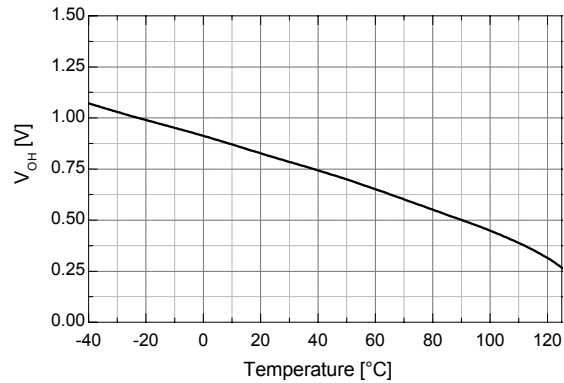
**Figure 13. Logic High Input Voltage vs. Temp.**



**Figure 14. Logic Low Input Voltage vs. Temp.**

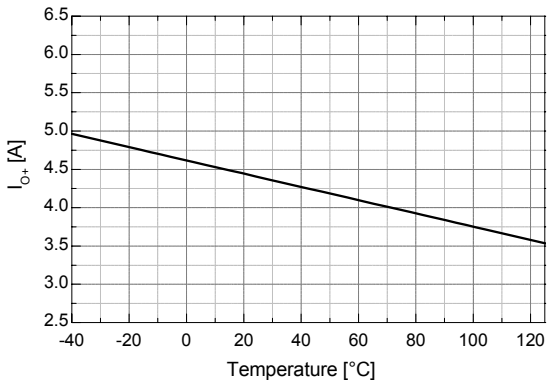


**Figure 15. Input Pull-down Resistance vs. Temp.**

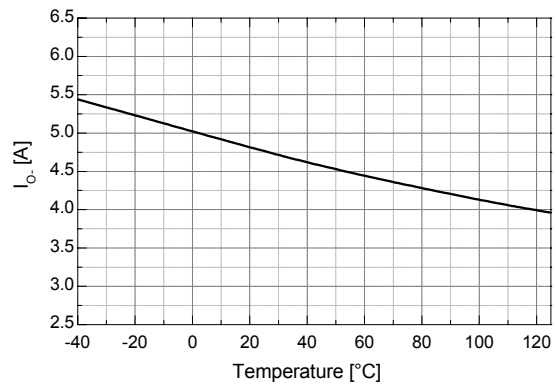


**Figure 16. High-Level Output Voltage vs. Temp.**

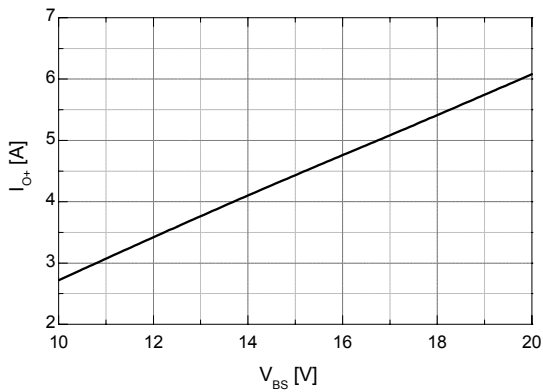
**Typical Characteristics** (Continued)



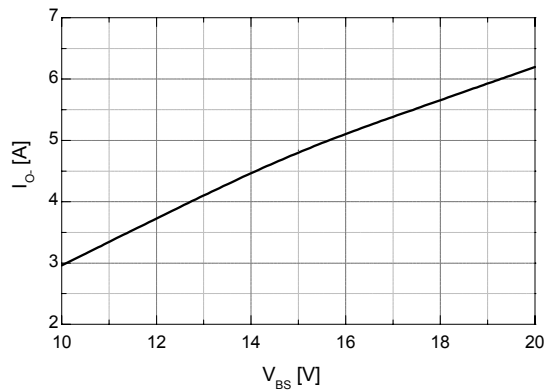
**Figure 17. Output High, Short-Circuit Pulsed Current vs. Temp.**



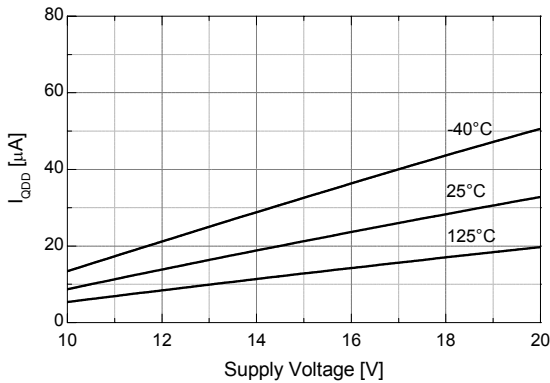
**Figure 18. Output Low, Short-Circuit Pulsed Current vs. Temp.**



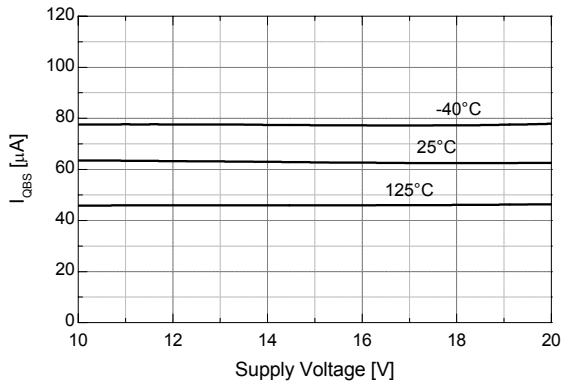
**Figure 19. Output High, Short-Circuit Pulsed Current vs. Supply Voltage**



**Figure 20. Output Low, Short-Circuit Pulsed Current vs. Supply Voltage**



**Figure 21. Quiescent  $V_{DD}$  Supply Current vs. Supply Voltage**



**Figure 22. Quiescent  $V_{BS}$  Supply Current vs. Supply Voltage**

### Switching Time Definitions

#### Timing Diagram

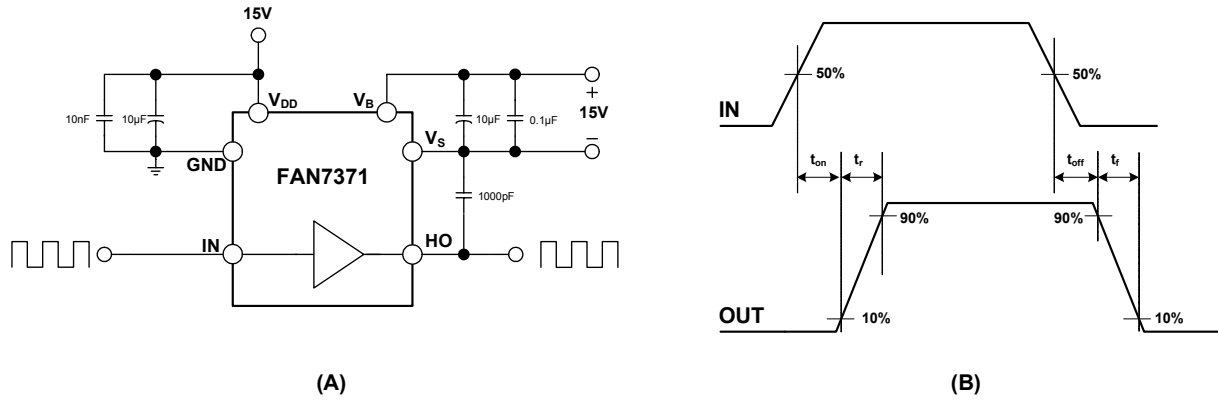
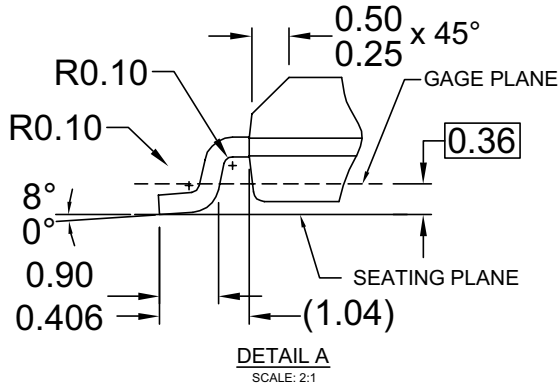
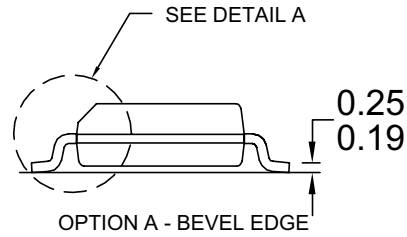
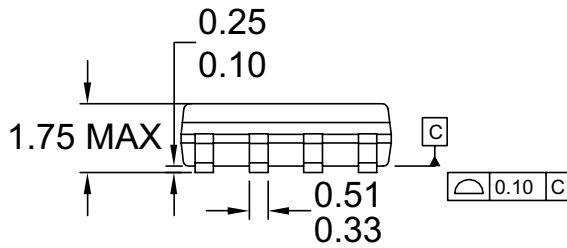
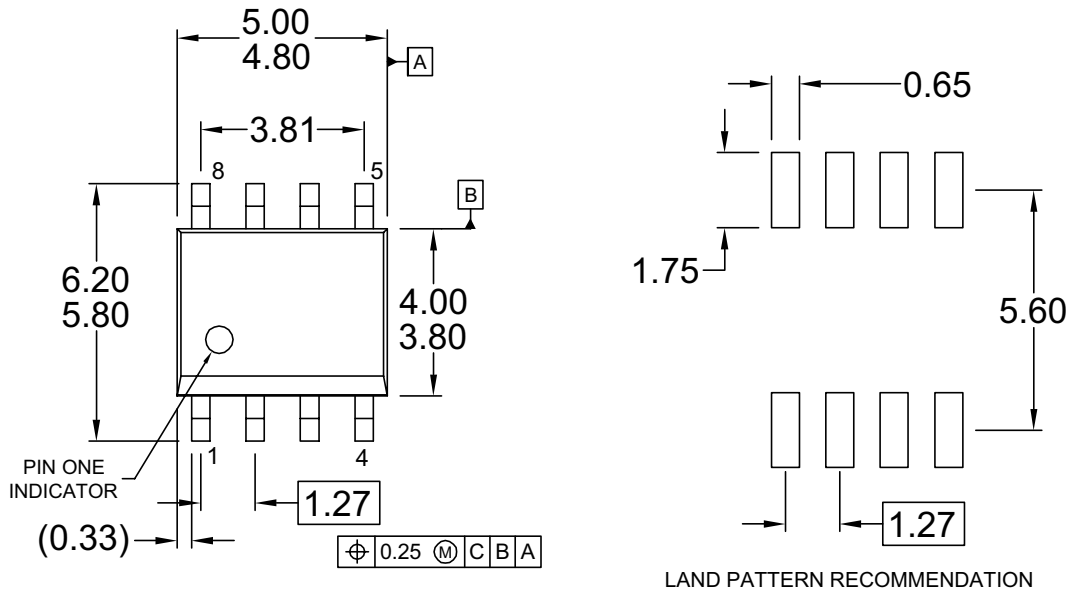


Figure 23. Switching Time Test Circuit and Waveform Definitions

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
- E) DRAWING FILENAME: M08AREV13

Figure 24. 8-Lead Small Outline Package (SOP)



**TRADEMARKS**

The following are registered and unregistered trademarks and service marks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

- |                          |                      |                            |                            |
|--------------------------|----------------------|----------------------------|----------------------------|
| ACEx®                    | Green FPS™           | Power247®                  | SuperSOT™-8                |
| Build it Now™            | Green FPS™ e-Series™ | POWEREDGE®                 | SyncFET™                   |
| CorePLUS™                | GTO™                 | Power-SPM™                 | The Power Franchise®       |
| CROSSVOLT™               | <i>i-Lo</i> ™        | PowerTrench®               | the <b>power</b> franchise |
| CTL™                     | IntelliMAX™          | Programmable Active Droop™ | TinyBoost™                 |
| Current Transfer Logic™  | ISOPLANAR™           | QFET®                      | TinyBuck™                  |
| EcoSPARK®                | MegaBuck™            | QST™                       | TinyLogic®                 |
| <b>F</b> ®               | MICROCOUPLER™        | QT Optoelectronics™        | TINYOPTO™                  |
| Fairchild®               | MicroFET™            | Quiet Series™              | TinyPower™                 |
| Fairchild Semiconductor® | MicroPak™            | RapidConfigure™            | TinyPWM™                   |
| FACT Quiet Series™       | MillerDrive™         | SMART START™               | TinyWire™                  |
| FACT®                    | Motion-SPM™          | SPM®                       | μSerDes™                   |
| FAST®                    | OPTOLOGIC®           | STEALTH™                   | UHC®                       |
| FastvCore™               | OPTOPLANAR®          | SuperFET™                  | UniFET™                    |
| FPS™                     | ®                    | SuperSOT™-3                | VCX™                       |
| FRFET®                   | PDP-SPM™             | SuperSOT™-6                |                            |
| Global Power Resource™   | Power220®            |                            |                            |

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

| Datasheet Identification | Product Status         | Definition   |
|--------------------------|------------------------|--|
| Advance Information      | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.   |
| Preliminary              | First Production       | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production        | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.   |
| Obsolete                 | Not In Production      | This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.                                      |

Rev. I31